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EXAMINER	
CURS, NATHAN M	

ART UNIT	PAPER NUMBER
2633	8

DATE MAILED: 04/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/621,009	YANG ET AL.	
	Examiner	Art Unit	
	Nathan Curs	2633	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 July 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3, 4 and 5*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1-13, 16-25, 27-33, 36, 37, and 40 are rejected under 35 U.S.C. 102(a) as being anticipated by Mokhtari et al. ("Bit-rate transparent electronic data regeneration in repeaters for high speed lightwave communication systems", Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on, Volume 2, 30 May-2 June 1999, pages 508-511 vol. 2)

Regarding claim 1, Mokhtari et al. disclose an apparatus, comprising: a fiber optic system including an electrical 3R function (page 508, col. 2, paragraph 3 and 4, and col. 2, paragraph 3); where this system includes a converter to convert an input optical signal to an original electrical signal (page 508, col. 2, paragraph 4); an identification unit receiving the original electrical signal (fig. 5 and page 509, col. 2, paragraph 1), generating a first signal corresponding to the original electrical signal delayed by a predetermined quantity of time and generating a second signal corresponding to the original electrical signal not delayed (fig. 5), comparing the first and second signals and forming a third signal in dependence upon the comparing of the first and second signals (fig. 5), detecting a bit rate in dependence upon the third signal (page 508, col. 1, paragraph 4 and page 509, col. 2, paragraphs 3 and 4); a clock generator generating a reference clock signal in dependence upon the detected bit rate and a recovery unit recovering an input clock signal and data from the input optical signal in

dependence upon the reference clock signal (fig. 3 and page 509, col. 1, paragraph 3); and wherein said identification unit further comprises: a first unit delaying said electrical signal, performing said exclusive-OR operation upon said first and second signals, and forming said third signal (fig. 5); and a second unit filtering said third signal, and detecting said bit rate in dependence upon a voltage level of said filtered signal (fig. 6 and page 509, col. 2, paragraph 4).

Regarding claim 2, Mokhtari et al. disclose an apparatus corresponding to an optical receiver receiving optical signals having a plurality of different bit rates (page 508, col. 1, paragraphs 3 and 4).

Regarding claim 3, Mokhtari et al. disclose that the bit rate of the input optical signal corresponds to a transmission rate (page 508, paragraphs 1, 3 and 4).

Regarding claim 4, Mokhtari et al. disclose an amplifier amplifying the original electrical signal received from the converter (page 508, col. 2, paragraph 4 to page 509, col. 1, paragraph 1).

Regarding claim 5, Mokhtari et al. disclose that the amplifier outputs the amplified electrical signal to the identification unit (page 508, col. 2, paragraph 4 to page 509, col. 1, paragraph 1; and fig. 1, fig. 3 and fig. 5).

Regarding claims 6 and 31, Mokhtari et al. disclose an apparatus, comprising: a fiber optic system including electrical 3R regeneration (page 508, col. 1, paragraph 3 and 4, and col. 2, paragraph 3); where this system includes an optoelectric converter to convert an input optical signal to an original electrical signal (page 508, col. 2, paragraph 4).

Regarding claims 7 and 32, Mokhtari et al. disclose an identification unit corresponding to a bit rate identification unit (fig. 3 and 5, and page 509, col. 2, paragraph 1).

Regarding claims 8 and 18, Mokhtari et al. disclose that the comparing performed by the identification unit corresponds to the identification unit performing an exclusive-OR logic operation upon the first and second signals (fig. 5).

Regarding claim 9, Mokhtari et al. disclose that the forming of the third signal performed by the identification unit corresponds to the identification unit forming the third signal in dependence upon the exclusive-OR logic operation performed upon the first and second signals (fig. 5).

Regarding claims 10 and 33, Mokhtari et al. disclose a first unit delaying the original electrical signal and performing the exclusive-OR operation upon the first and second signals and forming the third signal (fig. 5); and a second unit filtering the third signal, detecting the bit rate in dependence upon a voltage level of the filtered third signal (fig. 6 and page 509, col. 2, paragraph 4).

Regarding claims 11 and 37, Mokhtari et al. disclose that the filtering corresponds to low-pass filtering (page 509, col. 2, paragraph 4).

Regarding claim 12, Mokhtari et al. disclose a unit corresponding to a bit rate identification signal generator (fig. 3 and fig. 6 and page 509, col. 2, paragraph 4), where the filter output inherently corresponds to a bit rate identification signal.

Regarding claim 13, Mokhtari et al. disclose a unit corresponding to a bit rate deriving unit (fig. 6 and page 509, col. 2, paragraph 4), where the unit including the bank of oscillators inherently derives a bit rate by tuning the VCO to the bit rate, based on the output signal from the filter.

Regarding claims 16, 27, 29, and 36, Mokhtari et al. disclose that the clock generator and clock generation method comprise a plurality of oscillators generating clocking signals of different frequencies and selectively operating the oscillators to generate the reference clock

signal in dependence upon the bit rate detected by the identification unit (fig. 6 and col. 2, paragraph 4).

Regarding claim 17, Mokhtari et al. disclose a method, comprising: a fiber optic system including an electrical 3R function (page 508, col. 2, paragraph 3 and 4, and col. 2, paragraph 3); where this system includes a converter to convert an input optical signal to an original electrical signal (page 508, col. 2, paragraph 4); an identification unit receiving the original electrical signal (fig. 5 and page 509, col. 2, paragraph 1), generating a first signal corresponding to the original electrical signal delayed by a predetermined quantity of time and generating a second signal corresponding to the original electrical signal not delayed (fig. 5), comparing the first and second signals and forming a third signal in dependence upon the comparing of the first and second signals (fig. 5), detecting a bit rate in dependence upon the third signal (page 508, col. 1, paragraph 4 and page 509, col. 2, paragraphs 3 and 4); a clock generator generating a reference clock signal in dependence upon the detected bit rate and a recovery unit recovering an input clock signal and data from the input optical signal in dependence upon the reference clock signal (fig. 3 and page 509, col. 1, paragraph 3).

Regarding claims 19 and 25, Mokhtari et al. disclose receiving an original signal corresponding to an input optical signal (page 508, col. 1, paragraphs 3 and 4; and col. 2, paragraph 3), where this system includes a converter to convert an input optical signal to an original electrical signal (page 508, col. 2, paragraph 4); outputting two duplicate signals substantially equivalent to the electrical signal, the two duplicate signals corresponding to a primary signal and a secondary signal (fig. 5); and delaying the primary signal by the predetermined quantity of time (fig. 5 and page 509, col. 2, paragraph 1), and outputting a delayed primary signal corresponding to the first signal (fig. 5).

Regarding claim 20, Mokhtari et al. disclose a 3R regenerator with optoelectric conversion at the signal input (page 508, col. 2, paragraph 4), and disclose the first, second and third signals (fig. 5), where these three signal are inherently electrical for a 3R regenerator with optoelectric conversion.

Regarding claim 21 and 24, Mokhtari et al. disclose a method corresponding to receiving optical signals having a plurality of different bit rates (page 508, col. 1, paragraphs 3 and 4, and col. 2, paragraph 3).

Regarding claims 22 and 30, Mokhtari et al. disclose an original signal received corresponding to a plurality of original signals received (page 508, col. 1, paragraphs 3, 4, and 6), the recovering of the input clock signal and data from the original signal being performed for the plurality of original signals received (fig. 3 and page 509, col. 1, paragraphs 3 and 4), the plurality of original signals received having a respective plurality of different bit rates (page 508, col. 1, paragraphs 3, 4, and 6).

Regarding claim 23, Mokhtari et al. disclose recovering of the input clock signal and data from the original signal performed for a plurality of original signals received (fig. 2, fig. 3, page 509, col. 1, paragraphs 3, 4, and 5), the plurality of original signals received having a respective plurality of different bit rates (page 508, col. 1, paragraphs 3, 4 and 6).

Regarding claim 28, Mokhtari et al. disclose a 3R regenerator receiving an input optical signal (page 508, col. 2, paragraph 3), where this system includes a converter to convert an input optical signal to an original electrical signal (page 508, col. 2, paragraph 4); an identification unit receiving the original electrical signal (fig. 5 and page 509, col. 2, paragraph 1), generating a first signal corresponding to the original electrical signal delayed by a predetermine quantity of time and generating a second signal corresponding to the original electrical signal not delayed (fig. 5), forming a third signal by performing an exclusive-OR logic

operation upon the first and second signals (fig. 5), detecting a bit rate in dependence upon the third signal and a clock generator generating a reference clock signal in dependence upon the detected bit rate (fig. 3, fig. 6 and page 509, col. 2, paragraphs 3 and 4); and a recovery unit recovering an input clock signal and data from the input optical signal in dependence upon the reference clock signal (fig. 3 and page 509, col. 1, paragraph 3).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 15, 26, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mokhtari et al. ("Bit-rate transparent electronic data regeneration in repeaters for high speed lightwave communication systems", Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on, Volume 2, 30 May-2 June 1999, pages 508-511 vol. 2) in view of Uda et al. (European Patent Office Publication No. 0342010).

Regarding claims 15, and 35, Mokhtari et al. disclose two duplicate signals substantially equivalent to the original electrical signal, the two duplicate signals corresponding to a primary signal and a secondary signal (fig. 5); a delay unit receiving the primary signal, delaying the primary signal by the predetermined quantity of time, outputting the primary signal, the delayed primary signal corresponding to the first signal (fig. 5); and an operator unit performing the exclusive-OR logic operation upon the first and second signals (fig. 5 and page 509, col. 2, paragraph 1). Mokhtari et al. do not disclose a buffer unit receiving the original electrical signal and outputting two signals. Uda et al. disclose a digital signal regenerator, including a primary

signal and a secondary signal, delaying the primary signal, and an exclusive-OR logic operation upon the first and second signals (page 3, lines 17-21). Uda et al. also disclose input buffer amplifier amplifying the original electrical signal and outputting two duplicate signals (page 3, line 17). It would have been obvious to an artisan at the time of the invention to include a buffer unit, as taught by Uda et al., at the input of the Mokhtari et al. regenerator, to amplify the input signal and then output two duplicate signals directly to the compare circuit.

Regarding claim 26, Mokhtari et al. disclose a method, as described above, comprising: receiving an optical signal original signal using an optoelectric converter, converting the optic signal to an electrical signal, forming two duplicate signals and delaying one of the signals by a predetermined quantity of time. Mokhtari et al. do not disclose that the two duplicate signals are output from a buffer. Uda et al. also disclose input buffer amplifier amplifying the original electrical signal and outputting two duplicate signals (page 3, line 17). It would have been obvious to an artisan at the time of the invention to include a buffer unit, as taught by Uda et al., at the input of the Mokhtari et al. regenerator, to amplify the input signal and then output two duplicate signals directly to the compare circuit.

5. Claims 14, 34, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mokhtari et al. ("Bit-rate transparent electronic data regeneration in repeaters for high speed lightwave communication systems", Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on, Volume 2, 30 May-2 June 1999, pages 508-511 vol. 2) in view of Ishihara (US Patent No. 5557648).

Regarding claims 14, 34 and 38, Mokhtari et al. disclose a second unit comprising: a filter for filtering the signal output from the compare circuit, and determiner determining the bit rate in dependence upon the signal received from the filter (fig. 6; and page 509, col. 2,

paragraph 4). Mokhtari et al. also disclose that the filter and determining circuits that follow the compare circuit (fig. 3) are part of a phase-locked loop, but do not disclose an analog-to-digital converter. Ishihara discloses a phase lock loop including a determining circuit that has an analog-to-digital converter receiving a filtered signal and converting the filtered signal from an analog signal to a digital signal (fig. 23 and col. 15, lines 38-59). It would have been obvious to an artisan at the time of the invention to include the analog-to-digital converter, as taught by Ishihara, after the filter in the phase locked loop of Mokhtari et al., to digitize the filter output.

6. Claims 39 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mokhtari et al. ("Bit-rate transparent electronic data regeneration in repeaters for high speed lightwave communication systems", Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on, Volume 2, 30 May-2 June 1999, pages 508-511 vol. 2) in view of Ishihara (US Patent No. 5557648) as applied to claims 14, 34 and 38 above, and further in view of Uda et al. (European Patent Office Publication No. 0342010).

Regarding claim 39, Mokhtari et al. disclose two duplicate signals substantially equivalent to the original electrical signal, the two duplicate signals corresponding to a primary signal and a secondary signal (fig. 5); a delay unit receiving the primary signal, delaying the primary signal by the predetermined quantity of time, outputting the primary signal, the delayed primary signal corresponding to the first signal (fig. 5); and an operator unit performing the exclusive-OR logic operation upon the first and second signals (fig. 5 and page 509, col. 2, paragraph 1). Mokhtari et al. do not disclose a buffer unit receiving the original electrical signal and outputting two signals. Uda et al. disclose a digital signal regenerator, including a primary signal and a secondary signal, delaying the primary signal, and an exclusive-OR logic operation upon the first and second signals (page 3, lines 17-21). Uda et al. also disclose input buffer

amplifier amplifying the original electrical signal and outputting two duplicate signals (page 3, line 17). It would have been obvious to an artisan at the time of the invention to include a buffer unit, as taught by Uda et al., at the input of the Mokhtari et al. regenerator, to amplify the input signal and then output two duplicate signals directly to the compare circuit.

Regarding claim 40, Mokhtari et al. disclose that the clock generator and clock generation method comprise a plurality of oscillators generating clocking signals of different frequencies and selectively operating the oscillators to generate the reference clock signal in dependence upon the bit rate detected by the identification unit (fig. 6 and col. 2, paragraph 4).

Response to Arguments

7. Applicant's arguments filed 8 January 2004 have been fully considered but they are not persuasive.

Regarding claims 1, 17, 28, the applicant argues that the Mokhtari et al. reference does not disclose low-pass filtering, analyzing the resulting voltage level and determining the bit rate as disclosed by the applicant. However, Mokhtari et al. do disclose the limitations of the applicant's claims. The specification is not the measure of invention. Therefore, limitations contained in the specification cannot be read into the claims for the purpose of avoiding prior art. In fig. 6a of Mokhtari et al., the PLL receives a signal from the edge detector and outputs a clock signal to a delay and then to a decision circuit (see fig. 3 also). The signal input to the PLL from the edge detector of Mokhtari et al. is the same as the applicant's claimed "third signal" (see fig. 5 also), and the PLL then low pass filters this input signal (fig. 6a, element "Low Pass Filter"), this filtered signal is then input in the bank of VCO's, and a VCO is tuned to the bit rate of the system based on the filtered signal. Thus the PLL of Mokhtari et al. disclose the limitation of "detecting a bit rate in dependence upon the third signal" and "a clock generator

generating a reference clock signal in dependence upon the detected bit rate ", as well as "a second unit filtering said third signal" and "detecting said bit rate in dependence upon a voltage level of said filtered signal", where the filter signal represents the bit rate in order to tune the VCO to the proper frequency, and thus the filter signal represents detection of the bit rate.

Regarding claims 2-13, 16, 18-25, 27, 29-33, 36-37, and 40, the applicant argues that Mokhtari et al. do not disclose the limitations of these claims based on the argument that Mokhtari et al. do not disclose the limitations of corresponding independent claims 1, 17 and 28. As described above, Mokhtari et al. do disclose the limitations of claims 1, 17, and 28, and also disclose the limitations of claims 2-13, 16, 18-25, 27, 29-33, 36-37, and 40 as previously cited.

Regarding claims 15, 26, 35, and 39, the applicant argues that Uda et al. disclose extracting a timing wave having a predetermined bit rate from a received signal, which is different from the applicant's disclosure of detecting the bit rate of input optical signals having different bit rates. However, the teaching of Uda et al. cited by the examiner is the utility of the input buffer amplifier prior to comparison of the duplicate signals. The applicant claims that Uda et al. teaches an inverted input signal rather than a delayed signal with the original signal. However, Uda et al. does teach a delayed signal with the original signal, as the non-delayed signal is non-inverted as disclosed by Uda et al. In addition, the inverter at one amplifier output of Uda et al. does not teach away from the utility of amplifying the input signal prior to outputting two duplicate signals for the circuit of Mokhtari et al., where it would have been obvious to one of ordinary skill in the art at the time of the invention that the two duplicate signals of Mokhtari et al. could easily be maintained when applying the buffer amplifier teaching of Uda et al. by simply removing the inverter from the one buffer amplifier output when applying the buffer amplifier teaching of Uda et al. to the input of the edge detector circuit of Mokhtari et al.

Regarding claims 14, 34 and 38, the applicant argues that Ishihara teaches doubling the input frequency data and detecting the phase difference between the output of the doubler and that of a VCO output rather than disclosing a structure for low-pass filtering, analyzing the resulting voltage level and determining the bit rate. However, as described above, Mokhtari et al. disclose low-pass filtering, analyzing the resulting voltage level and determining the bit rate as claimed by the applicant in claims 1, 17 and 28. The teaching of Ishihara cited by the examiner is an analog-to-digital converter receiving a filtered signal and converting the filtered signal from an analog signal to a digital signal, as previously cited.

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Applicant is request to note that regarding claims 14, 34, 38, 39 and 40, the examiner modified the description of the structure of the 35 USC 103 combinations in the heading paragraphs of the rejections for these claims, due to typographical errors misrepresenting the claim dependencies for the rejections in the office action of 8 October 2003, where the reference of Uda et al. was unnecessarily included in the description of the combination of the rejection of claims 14, 34 and 38; the reference of Ishihara required due to claim dependency was omitted from the description of combination of the rejection of claims 39; and the dependency of claim 40 on claim 39 was not properly represented. However, the content of the specific claim rejections for these claims, based on the disclosure of Mokhtari et al. and the teachings of Uda et al. and Ishihara references as applicable to the Mokhtari et al. reference, remain unchanged.

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

9. Any inquiry concerning this communication from the examiner should be directed to N. Curs whose telephone number is (703) 305-0370. The examiner can normally be reached on M-F (from 9 AM to 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan, can be reached at (703) 305-4729. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

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